

IN THE SPECIFICATION

Please amend the specification at page 1, lines 4-11, as follows:

Cross-Reference to Related Applications

The present application is related to United States Patent Application Serial Number 10/764,150, entitled "Method and Apparatus for Reducing Leakage Current in a Read Only Memory Device Using Shortened Precharge Phase," (~~Attorney Docket No. Dudeck 1-4-32-5~~), and United States Patent Application Serial Number 10/764,152, entitled "Method and Apparatus for Reducing Leakage Current in a Read Only Memory Device Using Pre-Charged Sub-Arrays," (~~Attorney Docket No. Dudeck 2-5-33-6~~), each filed contemporaneously herewith and incorporated by reference herein.

Please amend the specification at page 7, lines 17-25, as follows:

ROM memory arrays typically use n-channel cell transistors. When p-channel transistors are used, the column precharge voltage would typically be 0 volts (ground) and the source ~~terminals~~ terminals of the p-channel transistors, connected to the source voltage bus, would typically be connected to V_{DD} . With conventional techniques, programmed, off-state (non-conductive state) memory cell transistors are biased with their source voltage (V_s) having the same voltage as their gate voltage (V_g). For n-channel transistors, V_s and V_g are at ground (0 volts); for P-channel transistors, V_s and V_g are at V_{DD} . While there might be some cases where the memory array does not operate at ground or V_{DD} levels, but at some other voltages, it would still be true that for an off-state transistor V_s equals V_g .